ASIC IP-core for encoding and decoding IEEE802.15.3c irregular LDPC codes

This Databrief introduces encoder and decoder of the irregular LDPC codes, (672,336), (672,504), and (672,588), as defined by the IEEE 802.15.3c working group[a].

The implementation provides: (a) High throughput. Data-rates higher than the raw data rates of single carrier (SC) PHY mode, and high speed interface (HSI) PHY mode; (b) Low-power consumption and logic controlled gated clocks; (c) High silicon utilization and reduced gate count; and (d) Low error rates with both fine and coarse signal quantization.

LDPC codes are linear block codes based on sparse parity-check matrices, that can be efficiently decoded using low-complexity *iterative* algorithms. In recent years LDPC based coding schemes became a preferable advanced channel coding solution, used in various standards and in IEEE 802.15.3c.

Overview

The $\mathcal{C}$**b**-LDPC-802.15.3cIrr is a high performance decoder and encoder, that features:

Pipeline architecture for maximal clock frequency and throughput in a given clock frequency. 4 clocks per decoding iteration.

Smart datapath multiplexing enables higher throughput determined by the *average* number of iterations. A codeword that needs more than average iterations benefits from codewords that need less iterations.

Decoder versions optimized for different applications and requirements, enable tradeoffs between gate count, throughput, and performance.

Features

- ✓ Belief-propagation iterative decoding
- ✓ Pipeline design, 4 clocks per-decoding-iteration
- ✓ Single clock synchronous design; registered inputs and outputs;
- ✓ Single-port memories only
- ✓ Portable to all ASIC technologies
- ✓ On-the-fly configuration, with each codeword, of code rate and maximal number of iterations to simplify the use with unequal error protection (UEP) MSC.
- ✓ Continuous monitoring of convergence enables early stop of iterations when a codeword is found
- ✓ Low power design. Dedicated logic gates the clock to parts of decoder when no data is available for decoding

[a] http://www.ieee802.org/15/

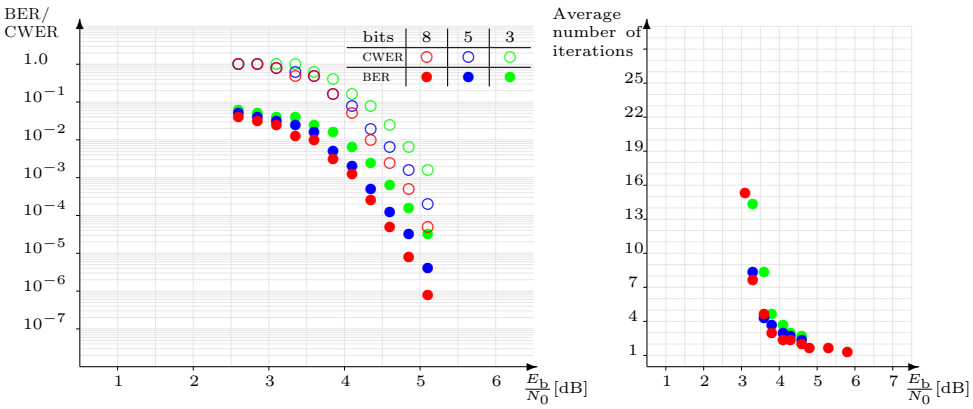

Figure 1: HDL simulation results for rate 7/8. The received analog signal is quantized with 8-bit ADC, 5-bit ADC and 3-bit ADC.

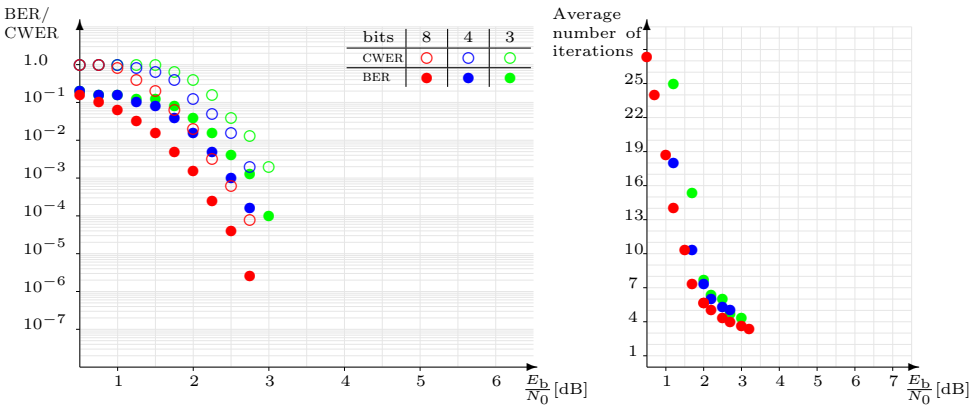

Figure 2: HDL simulation results for rate 1/2. The received analog signal is quantized with 8-bit ADC, 4-bit ADC and 3-bit ADC.

Performance

HDL simulation results are plotted in Figures 1 and 2. The bit error rate (BER), codeword error rate (CWER) and average number of iterations were simulated as a function of the SNR (E_b/N_0)[1], and for various analog-to-digital conversion (ADC) quantizations.

In all the simulations, the SNR estimation was *not* provided to the decoder. If the receiver provides SNR estimation, the performance improves.

The average number of iterations is the main limiting factor on the throughput. Knowing that it takes 4 clocks per-iteration, and knowing the number of clocks between two received codewords (throughput), one can use the 'average number of iterations' sub-plots to estimate the minimal SNR needed for a given BER.

For more simulation data please contact Continuous bits Ltd.

Deliverables

The items delivered with the LDPC decoder are:

✓ Full Datasheet

✓ Encoder and decoder HDL source code

✓ EDIF for FPGA testing

✓ HDL test-bench

✓ C/Matlab bit exact model of the decoder

✓ Support during integration and simulations

Related products

(a) Encoder and decoder for rate 14/15 LDPC (1440,1344) code.

(b) Samples to LLR mapper. The mapping is from multiple antenna samples, and for different modulation schemes.

[1] E_b is the codeword's energy divided by the number of *information-bits*. N_0 is the Gaussian noise power spectral density.

Revision History

Revision	Date	Changes
1.0	Nov. 1, 2008	First web publication