ASIC IP-core for decoding CMMB's LDPC codes

China Multimedia Mobile Broadcasting (CMMB)[1] LDPC decoder, implemented with Continuous-bits' innovative LDPC-decoder architecture. The implementation provides high data-rates, low power consumption, high silicon utilization, and reduced gate count, with low error rates.

Overview

LDPC codes are linear block codes based on sparse parity-check matrices, that can be efficiently decoded using iterative algorithms. Their near-channel-capacity performance, under low complexity iterative decoding algorithms, have made them very attractive for commercial applications. Indeed, in recent years LDPC based coding schemes became a preferable advanced channel coding solution, used in various industry standards.

This databrief introduces the implementation of an ASIC-IP for the decoding of CMMB LDPC codes, base on Continuous-bits' innovative LDPC-decoder architecture characterized by low complexity and low power.

Decoders for other standard (e.g., DVB-S2, IEEE 802.16e, IEEE 802.11n, IEEE 802.3an) and custom LDPC codes can also be implemented. Starting from a set of parity-check matrices, Continuous-bits Ltd. shall implement a decoder that is finely trimmed to your product needs, and deliver a HDL code that is easy to integrate and simulate.

Features

- ✓ 1/2 and 3/4 code rates supported
- ✓ One clock synchronous design; registered inputs and outputs; global asynchronous reset
- ✓ Portable to all FPGA and ASIC technology
- ✓ FPGA proven, maximal clock frequency on Altera Stratix and Xilinx Virtex is over 100 MHz
- ✓ Internal double buffer for continuous decoding with maximal efficiency
- ✓ On-the-fly configuration of the maximal number of iterations
- ✓ Continuous monitoring of convergence enables early stops the iterations when a codeword is found
- ✓ Available as VHDL and Verilog codes
- ✓ Low power design.

[1] http://www.cmmb.org.cn

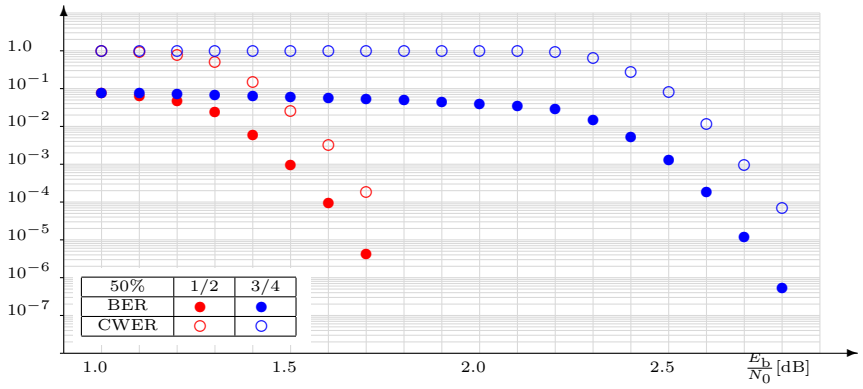

Figure 1: Bit error rate, •, and codeword error rate, ∘, for code rate 1/2 and code rate 3/4. The minimal codeword rate (bits per second) is determined by the configured maximal number of iteration. In this figure the minimal codeword rate is 50% of the IP-core clock frequency

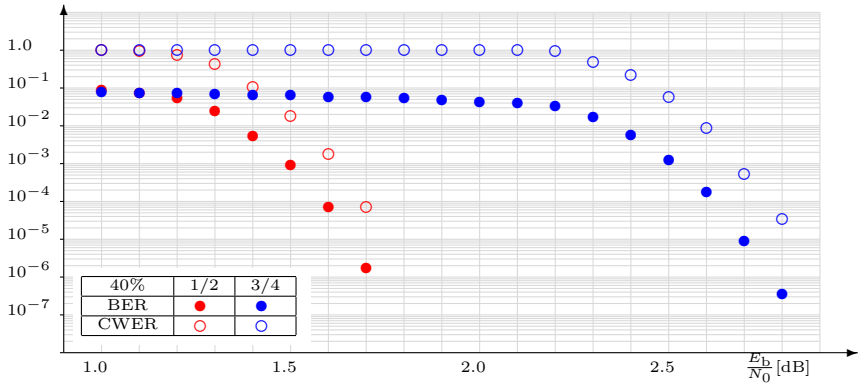

Figure 2: Bit error rate, •, and codeword error rate, ∘, for code rate 1/2 and code rate 3/4. The minimal codeword rate (bits per second) is determined by the configured maximal number of iteration. In this figure the minimal codeword rate is 40% of the IP-core clock frequency

Performance

The bit error rate (BER) and codeword error rate (CWER) are plotted in Figures 1 and 2. The two figures differs in the configured maximal number of decoding iterations. Lower number of iterations enables higher data rate, more iterations result in lower BER.

Deliverables

The items delivered with a LDPC decoder are:

✓ Full Datasheet

✓ Decoder HDL source code

✓ Test-bench (Matlab vs.HDL source code and script)

✓ Support during integration and simulations

Revision History

Revision	Date	Changes
1.0	May 2, 2008	First web publication
1.01	June 6, 2008	Minor typo corrections