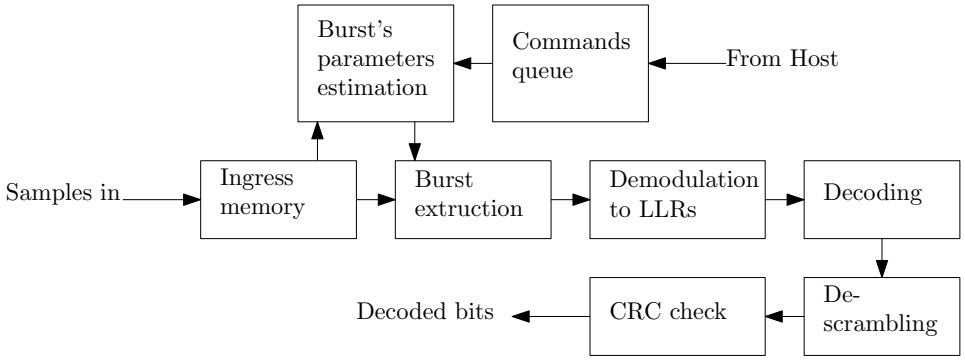
ASIC/FPGA IP-core for high-throughput decoding of DVB-RCS

This Databrief introduces a high-performance, high-throughput, and Low-power demodulator IP-core, compatible with ETSI EN 301 790 v1.4.1, *DVB interaction channel for satellite distribution systems*[1].

Features

- ✓ MF-TDMA, multi-frequency time division multiple access, burst mode
- ✓ Multichannel, simultaneous demodulation several bursts
- ✓ Up to 10% of symbol rate, frequency offset compensation
- ✓ Configurable burst arrival time window
- ✓ Excellent performance at low SNR
- ✓ Turbo and Viterbi+Reed-Solomon decoders
- ✓ On-the-fly configuration, per-decoded burst
- ✓ Channel status monitoring
- ✓ Decoding status (decoder convergence, CRC)
- ✓ Low power design:
- ✓ Single clock synchronous design
- ✓ Portable to all ASIC and FPGA technologies

[1] Some limitations apply, and depend on the IP-core configuration



Deliverables

✓ Simulation bit-exact model (Matlab MEX file, shared library, or PLI/VPI).

✓ RTL (for ASIC) or post-fit netlist (for FPGA)

✓ Test bench

✓ Integration guidelines document

✓ Support during simulations, integration, and backend.

Revision History

Revision	Date	Changes
1.0	Jan. 1, 2019	First publication.