

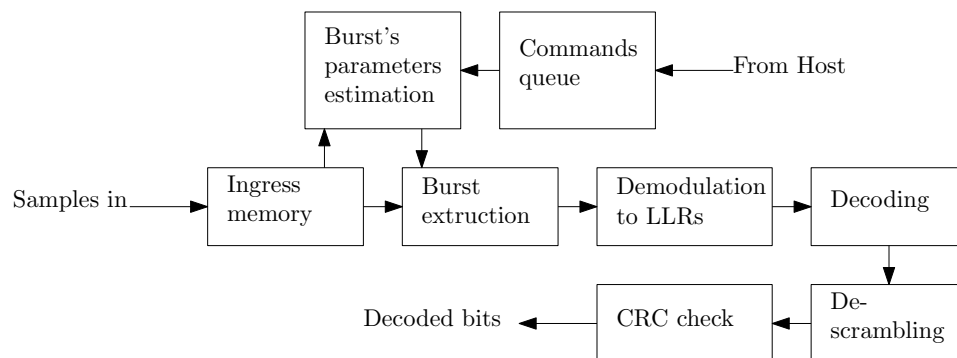
## ASIC/FPGA IP-core for high-throughput decoding of DVB-RCS

This Databrief introduces a high-performance, high-throughput, and Low-power demodulator IP-core, compatible with ETSI EN 301 790 v1.4.1, *DVB interaction channel for satellite distribution systems*<sup>1</sup>.

Features	
✓ MF-TDMA, multi-frequency time division multiple access, burst mode	✓ Turbo and Viterbi+Reed-Solomon decoders
✓ Multichannel, simultaneous demodulation several bursts	✓ On-the-fly configuration, per-decoded burst
✓ Up to 10% of symbol rate, frequency offset compensation	✓ Channel status monitoring
✓ Configurable burst arrival time window	✓ Decoding status (decoder convergence, CRC)
✓ Excellent performance at low SNR	✓ Low power design:
	✓ Single clock synchronous design
	✓ Portable to all ASIC and FPGA technologies

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<sup>1</sup>Some limitations apply, and depend on the IP-core configuration



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## Deliverables

- ✓ Simulation bit-exact model (Matlab MEX file, shared library, or PLI/VPI).
- ✓ RTL (for ASIC) or post-fit netlist (for FPGA)
- ✓ Test bench
- ✓ Integration guidelines document
- ✓ Support during simulations, integration, and backend.

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## Revision History

Revision	Date	Changes
1.0	Jan. 1, 2019	First publication.

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