

## ASIC IP-core for high-throughput decoding of DVB-S2/S2X, and DVB-RCS/RCS2

This Databrief introduces a high-performance, high-throughput (several Gpbs), and Low-power FEC IP-core<sup>1</sup>, that can be configured on-the-fly as:

DVB-S2/S2X LDPC decoder

or as

*Six* independent DVB-RCS/RCS2 Turbo decoders

Features	
✓ On-the-fly configuration, with each codeword:	✓ Indications on the number iterations done, early-convergence, and SNR
(a) LDPC/Turbo	✓ Low power design:
(b) All DVB-S2/S2X code rate (including Low-SNR)	(a) Gated-clock registers and FF
(c) Turbo interleaver parameters and codeword length per RCS/RCS2 decoder	(b) All memories <code>cs</code> port is negated on clocks not used to access the memory
(d) Maximal number of iterations.	(c) Continuous monitoring of convergence enables early stop of iterations when a codeword is found, or earlier if instructed due to system considerations.
✓ 500MHz clock with RAD-hard cells (TSMC 65LP)	(d) <code>idle</code> signal enables powering-off the whole IP-core
✓ Belief-propagation iterative decoding (floating-point performance)	✓ Single clock synchronous design
✓ Single-port memories, external to the IP-core	✓ All IP-core inputs and outputs are registered
✓ Options for synchronous or asynchronous reset	✓ Portable to all ASIC and FPGA technologies
✓ Efficient HW utilization ( $\approx 1$ )	

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<sup>1</sup>The IP-core can be shipped with additional support of the following standards: (a) DVB-T2 (including DVB-T2-Lite) (b) DMB-T (GB20600-2006) (c) CMMB

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## Deliverables

- ✓ Simulation bit-exact model (Matlab MEX file, shared library, or PLI/VPI).
- ✓ RTL (for ASIC) or post-fit netlist (for FPGA)
- ✓ Test bench
- ✓ Integration guidelines document
- ✓ Support during simulations, integration, and backend.

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## Revision History

Revision	Date	Changes
1.0	Jan. 1, 2016	First publication.

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