ASIC IP-core for high-throughput decoding of DVB-S2/S2X, and DVB-RCS/RCS2

This Databrief introduces a high-performance, high-throughput (several Gpbs), and Low-power FEC IP-core[1], that can be configured on-the-fly as:

DVB-S2/S2X LDPC decoder

or as

Six independent DVB-RCS/RCS2 Turbo decoders

Features

- ✓ On-the-fly configuration, with each codeword:
  - (a) LDPC/Turbo
  - (b) All DVB-S2/S2X code rate (including Low-SNR)
  - (c) Turbo interleaver parameters and codeword length per RCS/RCS2 decoder
  - (d) Maximal number of iterations.
- ✓ 500MHz clock with RAD-hard cells (TSMC 65LP)
- ✓ Belief-propagation iterative decoding (floating-point performance)
- ✓ Single-port memories, external to the IP-core
- ✓ Options for synchronous or asynchronous reset
- ✓ Efficient HW utilization (≈ 1)
- ✓ Indications on the number iterations done, early-convergence, and SNR
- ✓ Low power design:
  - (a) Gated-clock registers and FF
  - (b) All memories `cs` port is negated on clocks not used to access the memory
  - (c) Continuous monitoring of convergence enables early stop of iterations when a codeword is found, or earlier if instructed due to system considerations.
  - (d) `idle` signal enables powering-off the whole IP-core
- ✓ Single clock synchronous design
- ✓ All IP-core inputs and outputs are registered
- ✓ Portable to all ASIC and FPGA technologies

[1]The IP-core can be shipped with additional support of the following standards: (a) DVB-T2 (including DVB-T2-Lite) (b) DMB-T (GB20600-2006) (c) CMMB

Deliverables

✓ Simulation bit-exact model (Matlab MEX file, shared library, or PLI/VPI).

✓ RTL (for ASIC) or post-fit netlist (for FPGA)

✓ Test bench

✓ Integration guidelines document

✓ Support during simulations, integration, and backend.

Revision History

Revision	Date	Changes
1.0	Jan. 1, 2016	First publication.