ASIC IP-core for high-throughput LDPC encoding and decoding of DVB-T2/S2/S2X, and DMB-T

This Databrief introduces a high-performance, high-throughput, and Low-power LDPC encoding and decoding IP-cores.
Any combination of the following standards can be integrated in one IP-core instance:

(a) DVB-T2 (including DVB-T2-Lite)

(b) DVB-S2

(c) DVB-S2X (all modcodes, including Low-SNR)

(d) DMB-T[1] (GB20600-2006)

(e) CMMB[1]

Performance and throughput vs. gate-count can be trimmed according to customer needs.

Features

- ✓ Portable to all ASIC and FPGA technologies
- ✓ On-the-fly configuration, with each codeword, of code rate and maximal number of iterations
- ✓ Belief-propagation iterative decoding (floating-point performance)
- ✓ Single clock synchronous design
- ✓ All IP-core inputs and outputs are registered
- ✓ Single-port memories, external to the IP-core
- ✓ Options for synchronous or asynchronous reset
- ✓ Efficient HW utilization (≈ 1)
- ✓ Indications on the number iterations done, early-convergence, and SNR
- ✓ Low power design:
  - (a) Gated-clock registers and FF
  - (b) All memories `cs` port is negated on clocks not used to access the memory
  - (c) Continuous monitoring of convergence enables early stop of iterations when a codeword is found, or earlier if instructed due to system considerations.
  - (d) `idle` signal enables powering-off the whole IP-core

[1] Decoding only

Deliverables

✓ Simulation bit-exact model (Matlab MEX file, shared library, or PLI/VPI).

✓ RTL (for ASIC) or post-fit netlist (for FPGA)

✓ Test bench

✓ Integration guidelines document

✓ Support during simulations, integration, and backend.

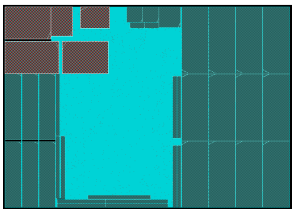
Customization of the LDPC IP-core

Different users have different needs. Not all aim for the floating-point performance with multi-Gbps throughput. Some just need a small gate-count, midrange throughput, and reasonable performance over AWGN.

The following steps demonstrate the customization process:

1. Continuous-bits delivers a simulation model of the decoder, with user control over HW internal parameters.
2. The user simulates with his channel models, and obtains the performance dependence on the HW parameters, and chooses the parameters most suitable for him.
3. Based, on user's selected parameters, the RTL parameters are determined, and the IP-core is generated.

IP-core customization is not for every user. Use this option if you have special requirements.



'Floating-point performance' implementation of the IP-core in SMIC 65LP. Erased areas on the top-left corner, are not part of the core.

Revision History

Revision	Date	Changes
0.1	Feb. 1, 2009	First publication
0.2	May. 10, 2012	Added DMB-T and CMMB
1.0	July. 28, 2013	Added IP-core image and DVB-S2X Evo. First web publication
1.1	Jan. 1, 2016	Change DVB-Sx to DVB-S2X. Explicitely state support of Low-SNR rates.